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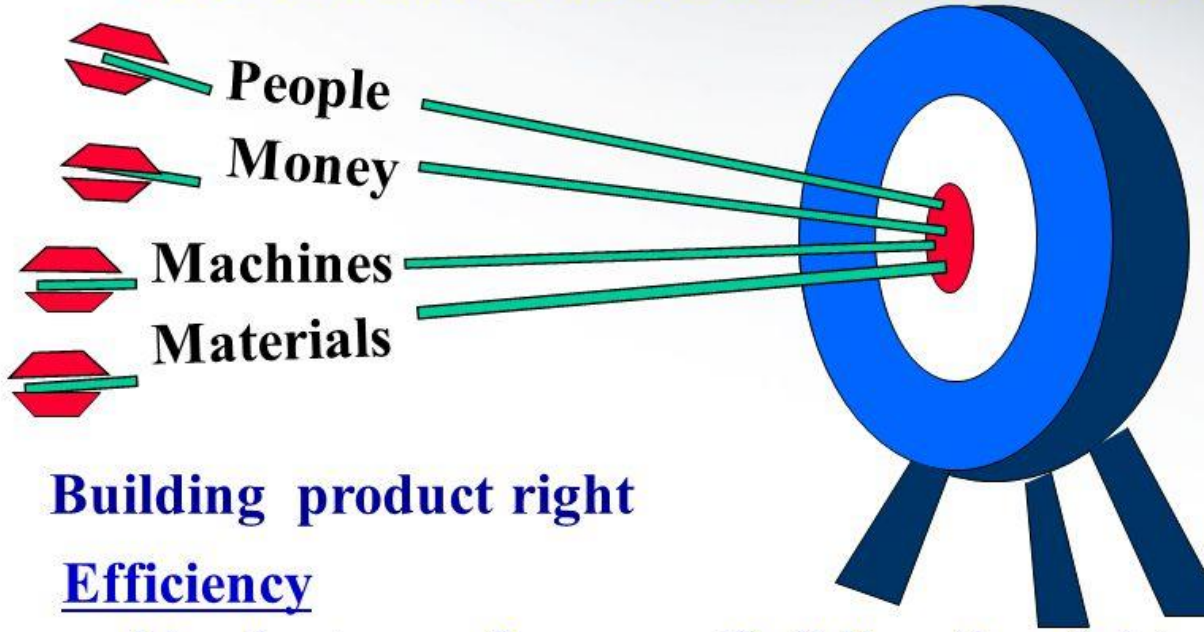
UNIVERSAL TEST CHIP

HI RELIABILITY PACKAGES AND THE FUTURE

- Manufacturing has become generic due to automation
- EDA Tools are closing the gap between concept of design vs actual, actual vs validation, validation vs tested, characterize vs actual
- Industry focus on manufacturability and centering of distribution where the predicted and the actual align: Sound modeling and simulation
- What is trailing behind is the way we validate reliability and PEM Quals
- Future is a few suppliers with process optimized, high volume tailored manufacturing capabilities, processes centered around highest possible efficiency and yield, dialed into that process, not necessarily a subset of a lot tailored for mil/aero or radiation lot.

Verification Vs. Validation

- Two questions
  - Are we building the right product ? => Validation
  - Are we building the product right ? = > Verification



Building product right

Efficiency

making best use of resources in achieving goals

Building the right product

Effectiveness

choosing effective goals and achieving them

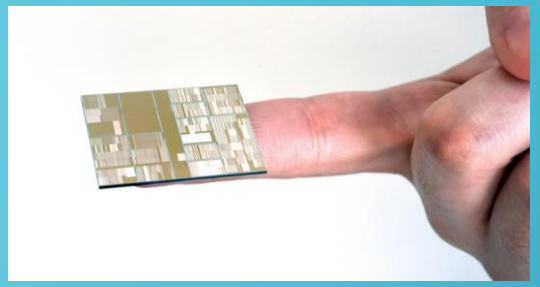
RELIABILITY: WHAT IS IT?

- An understanding of long term performance
- The functioning of a chip and its carrier/package
- Todays device Qual misses the point in terms of process deviation, process performance, process optimization.
- Current package Qual plan may not be able to catch the aberration or the manufacturability problem caused in a manufacturing process.
- Today's Qual is Pass/Fail

QUALIFICATION TODAY

- Hit or miss
- Relates to THAT particular distribution
- Peak performance or max performance not evaluated
- Thermal regulations not being mapped
- Only looking at life cycles of process
- Looking at reliability of a process versus what is the optimized process tailored and dialed into the design
- Equipment manufacturers consolidation: test, wire bond, die attach,

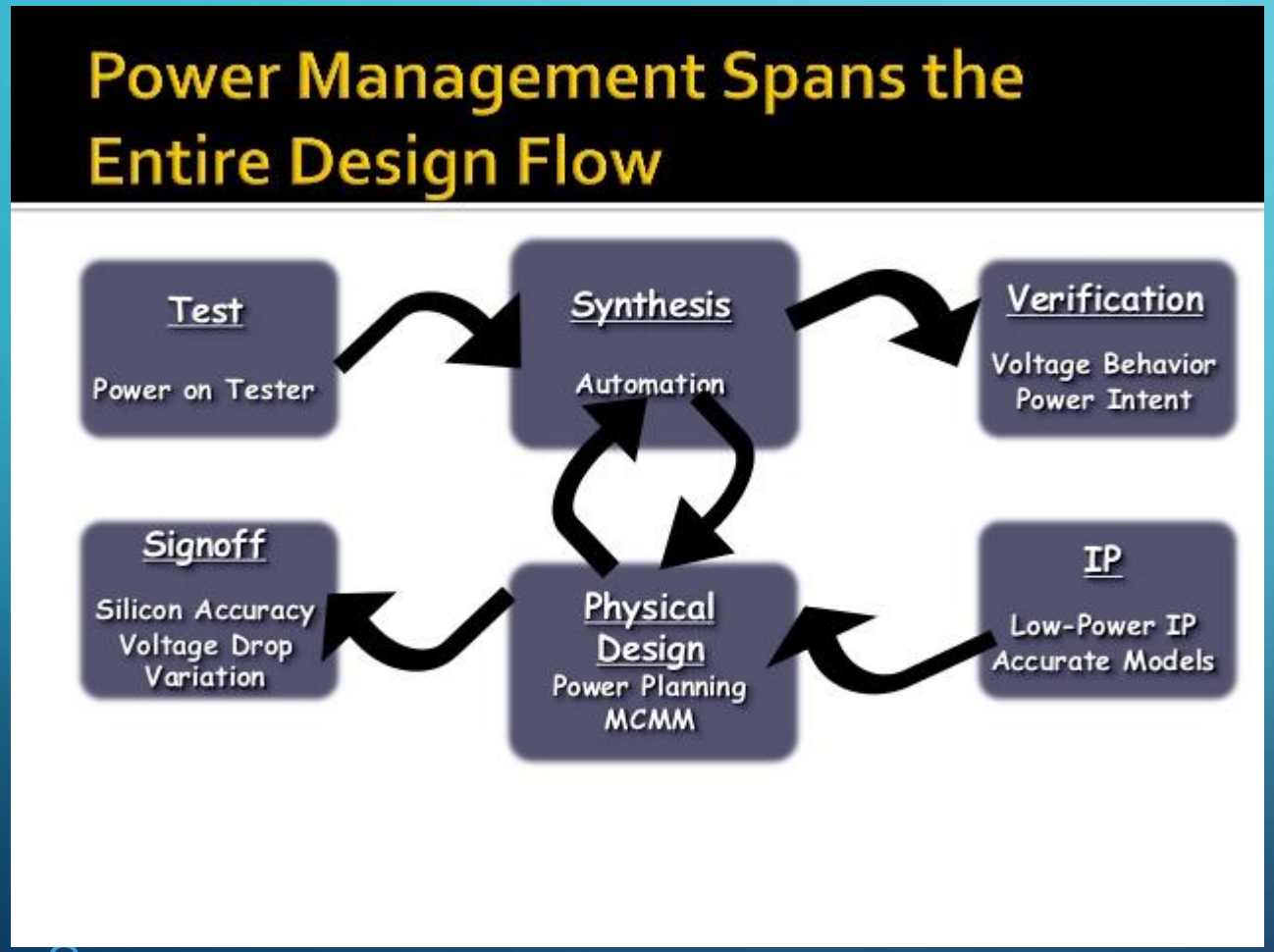
UNIVERSAL TEST CHIP
TWO PHASE PROJECT



- PHASE 1: Test Chip and Package
- Design
- Layout
- Documentation

- PHASE 2: Fabrication of die and package
- Wafer fab of die
- Tooling and procurement of packages
- Test program development
- Reliability Study

ALIGN FOR THE FUTURE: BENCHMARK STRATEGY

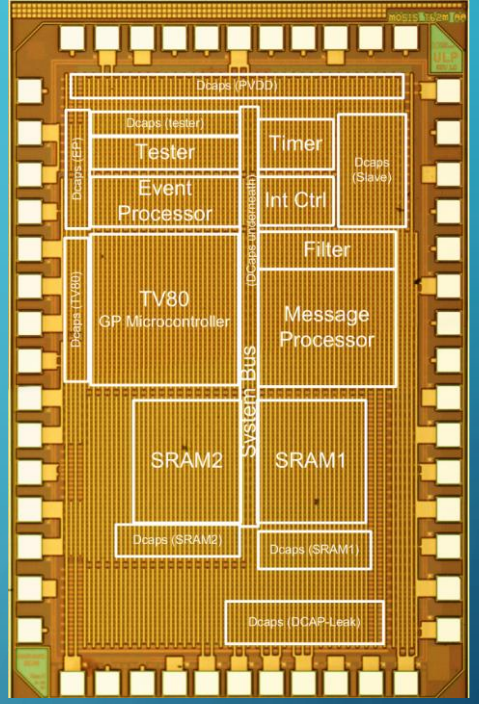


- Test circuit that is capable of quick indicators and assessment tools for reliability performance, defect density , validation, performance optimization, power draw, how much leakage there is, how much power is generated, how much leakage changes over time.
- Test package that is capable of performance in terms of connectivity, conductance, benchmark resistant paths in terms of vias, not just pass fail

WHAT'S IT ALL ABOUT: RELIABILITY PERFORMANCE INDICATORS

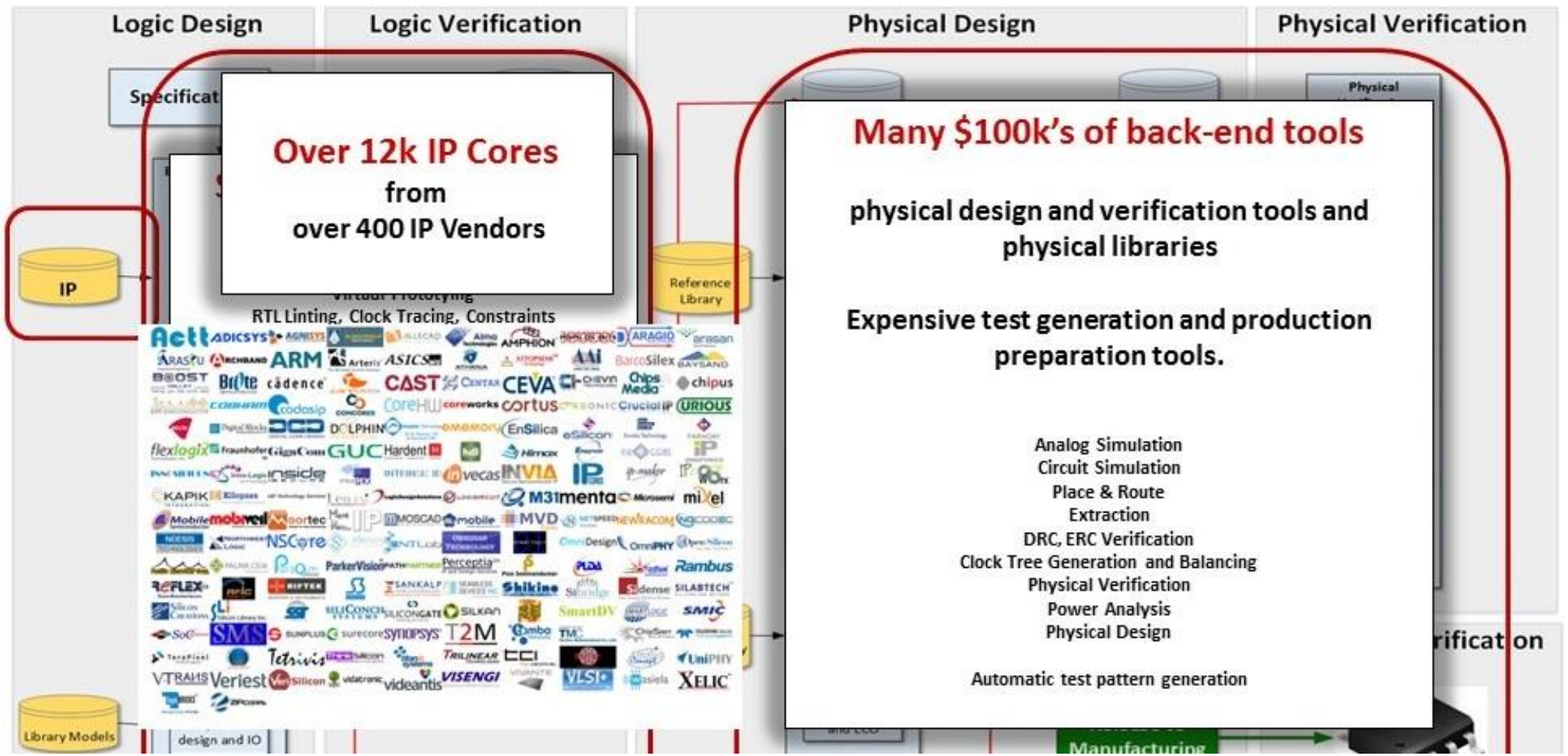
- Speed
- Performance
- Compaction density
- Power
- Density
- Infancy
- Thermal regulation
- Junction management
- Junction performance
- Substrate optimization
- Latency and leakage

WHAT IS THE PROPOSITION…EXACTLY?



- Create benchmark circuits and substrates (worse case scenarios)
- Standardized stressing techniques
- Standardized evaluation parameters
- Standardized test parameters and platforms

- Thermal mapping
- Design for manufacturing
- Cover all nodes- start at 90nm
- Form factor optimization
- Agree on what the chip will have: logic, PLL, RF, processor, memory, filters, switches, etc.

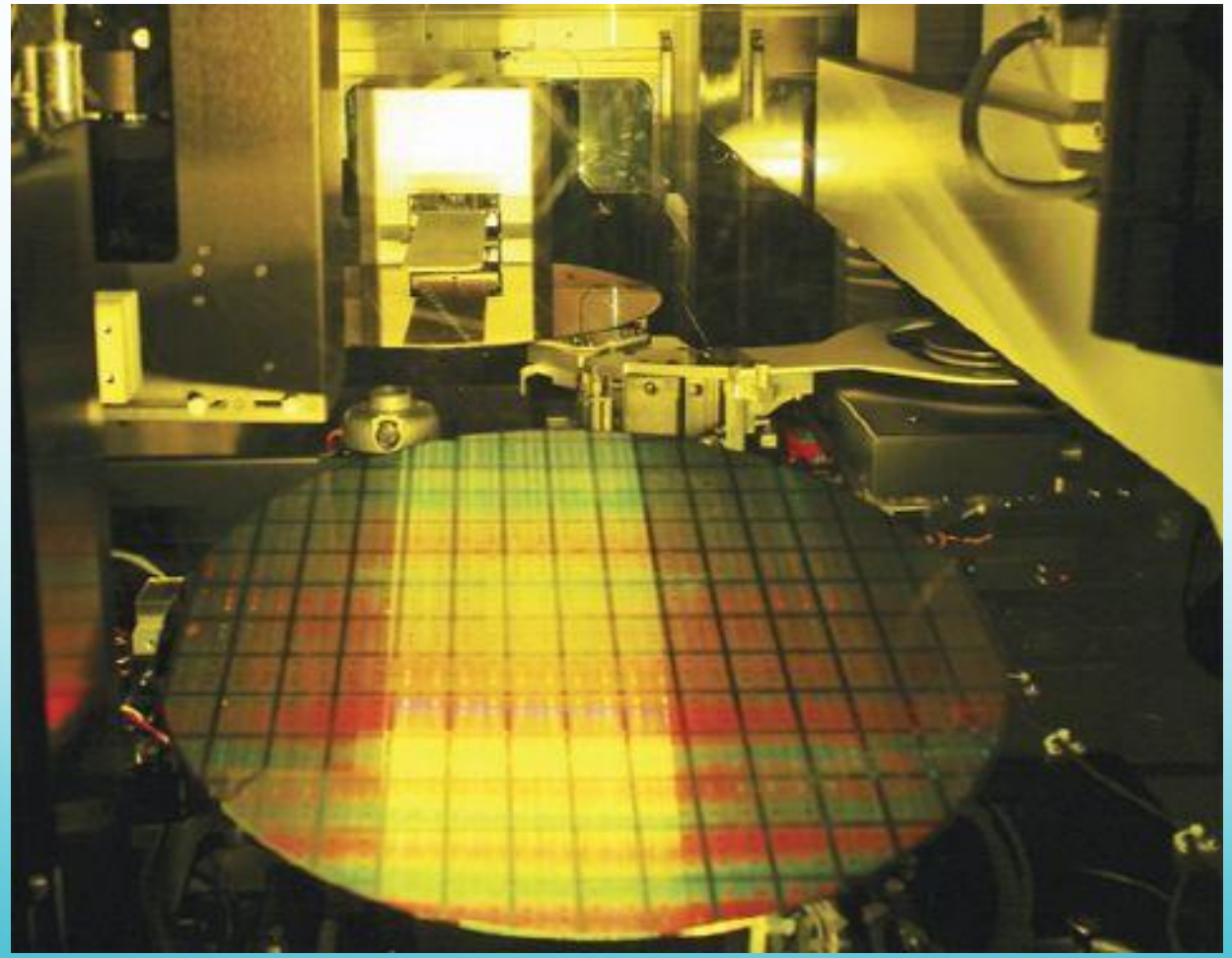

Logic Design
Logic Verification
Physical Design
Physical Verification
Specificat
IP
Library Models
design and IO
RTL Linting, Clock Tracing, Constraints
Reference Library
Physical
Over 12k IP Cores
from
over 400 IP Vendors
Many $100k's of back-end tools
physical design and verification tools and physical libraries
Expensive test generation and production preparation tools.
Analog Simulation
Circuit Simulation
Place & Route
Extraction
DRC, ERC Verification
Clock Tree Generation and Balancing
Physical Verification
Power Analysis
Physical Design
Automatic test pattern generation
Manufacturing

WHAT IS THE FUTURE?

- Relook at lot Quals and lot validation- has good intent- but what value does it add?
- Future: Integration of manufacturers, consolidation of foundries, limited foundry resources, mainstream production availability of IC assemblers, resource and material manufacturers consolidation

THE UNIVERSAL CONSORTIUM

- Optimized parameter screening of a production lot vs standard Qual
- Create a matrix of foundry, package type, assembly house
- Cloud pool data to share with the industry on all reliability and screening
- Impact globally saving millions for the DOD and Military customers
- Control, predict, screen and yield latency parameters such as thermal, leakages, inductance control – outcome is ultra high reliability that far exceeds the current qual life cycle
- Leading this charge today: Commercial space and automotive. No failures!

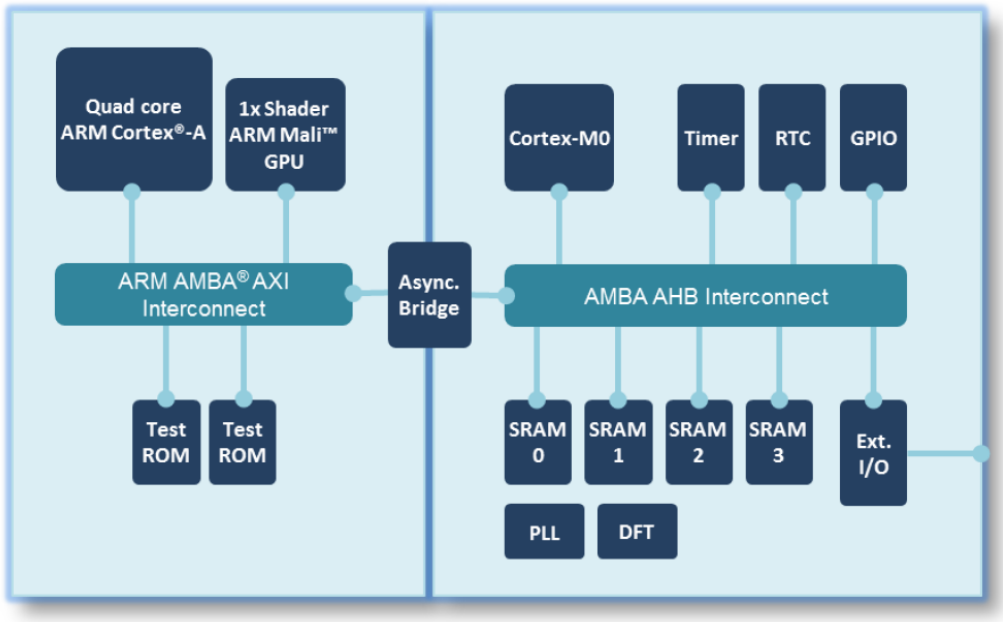


UTILIZE OUR IP FOR SHUTTLE WAFERS AT ANY TECHNOLOGY NODE

Universal test chip design can go to any foundry

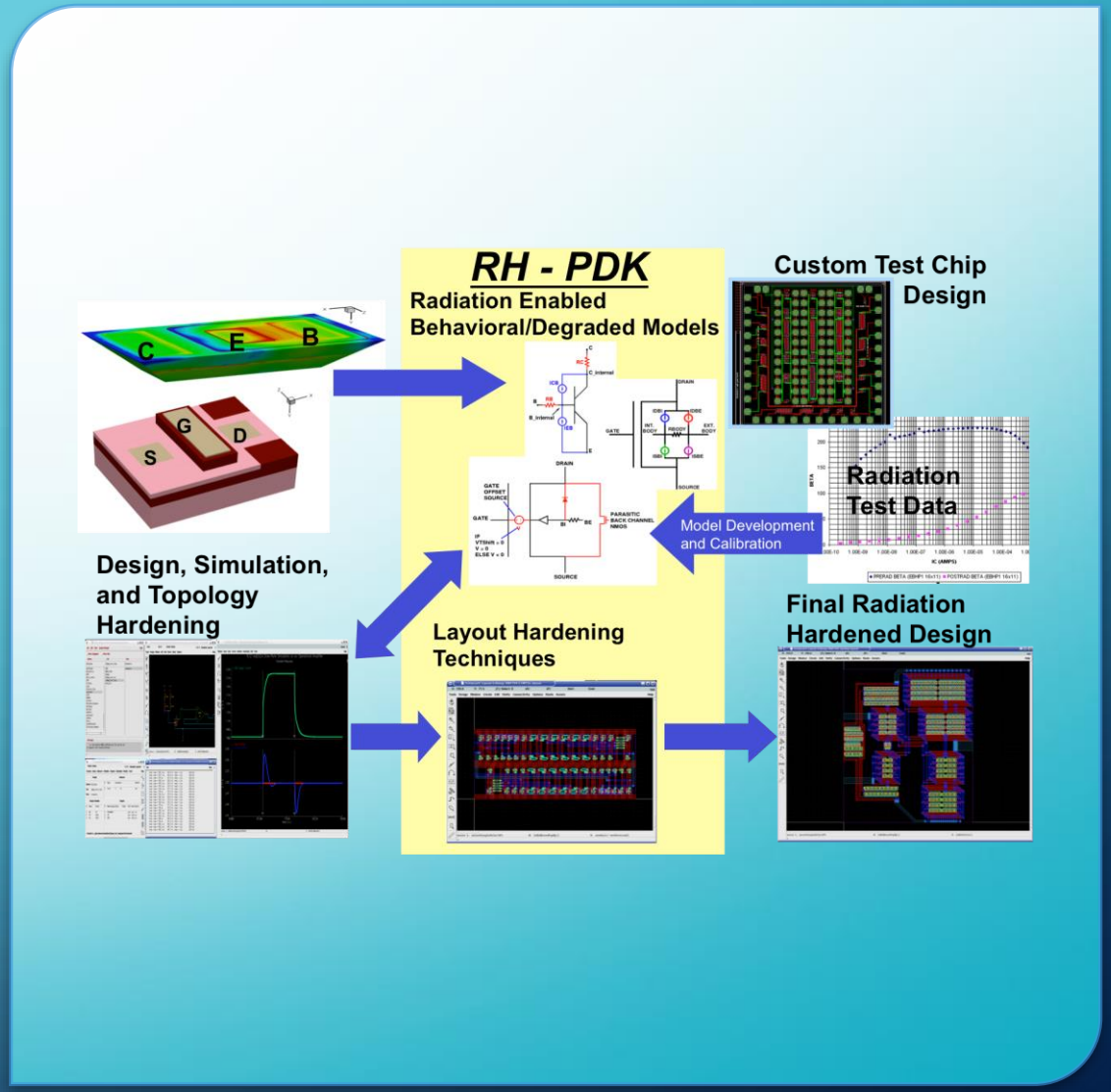
Stakeholders agree on design

Test Chip Architecture



- "Simple" silicon qualification test chip structure
  - Enables PPA benchmark testing on 10nm silicon
  - Manageable test chip complexity
- Real application CPU configuration
  - Quad core Artemis cluster
  - Power management
  - Production DFT structures
- Simplified GPU configuration
  - Single Mali shader core and top level
  - Demonstrates achievable PPA for larger configurations

STAKEHOLDERS AGREE ON STRESS DATA AND ANALYTICS



SHARED DATA BASE

MOVING FORWARD…….

1

Time for a fresh thought process on how we do conventional reliability and Quals that have no bearing on the physical product being used

2

It is an acceptance criteria not a criterion that necessarly validates a production lot

3

No more cherry picking for a high rel lot – utilize a main stream lot based on test results, not adding test latency

CONCLUSION

1. Looking for stakeholders and consortium members to outline design and package type
2. Road map for stress and reliability parameters
3. Designers, IP, Foundries, Package types, assembly and test house in place
4. First round funding

Thank you

Marti McCurdy

Beverly Marketing Management